

Equalized block

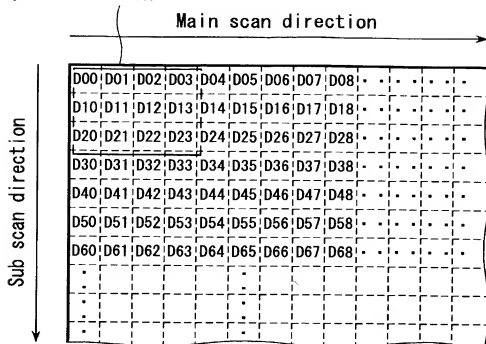


FIG. 1A

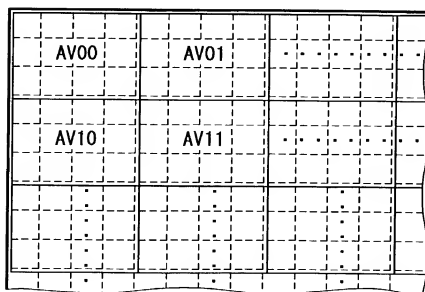


FIG. 1B

Equalizing start position

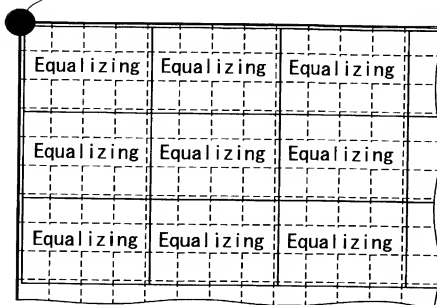


FIG. 2A

Equalizing start position

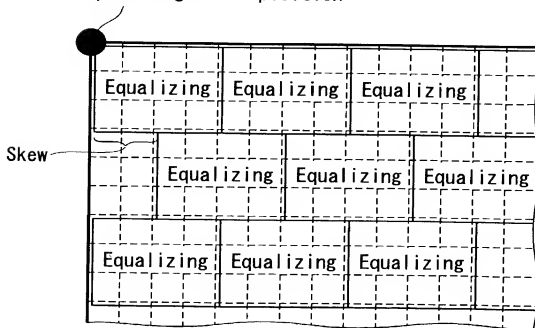


FIG. 2B

Equalizing start position

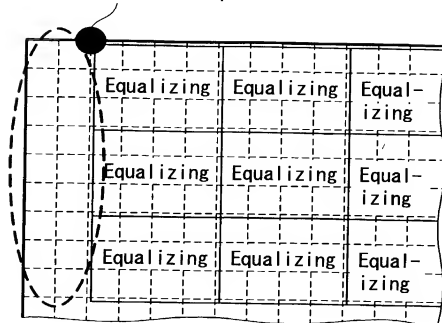


FIG. 3A

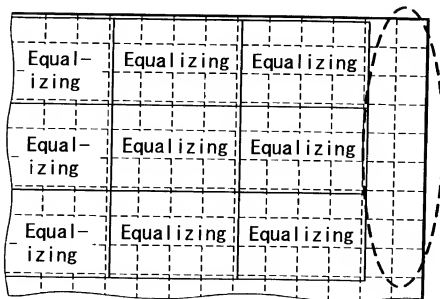


FIG. 3B

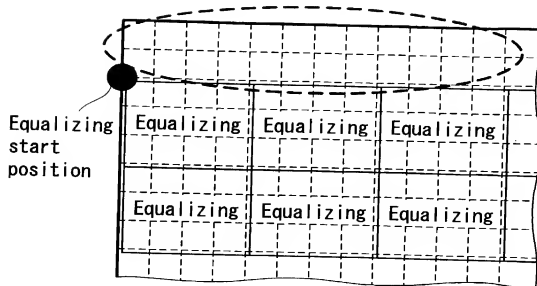


FIG. 3C

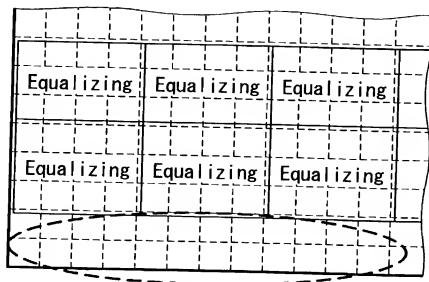


FIG. 3D



FIG. 4

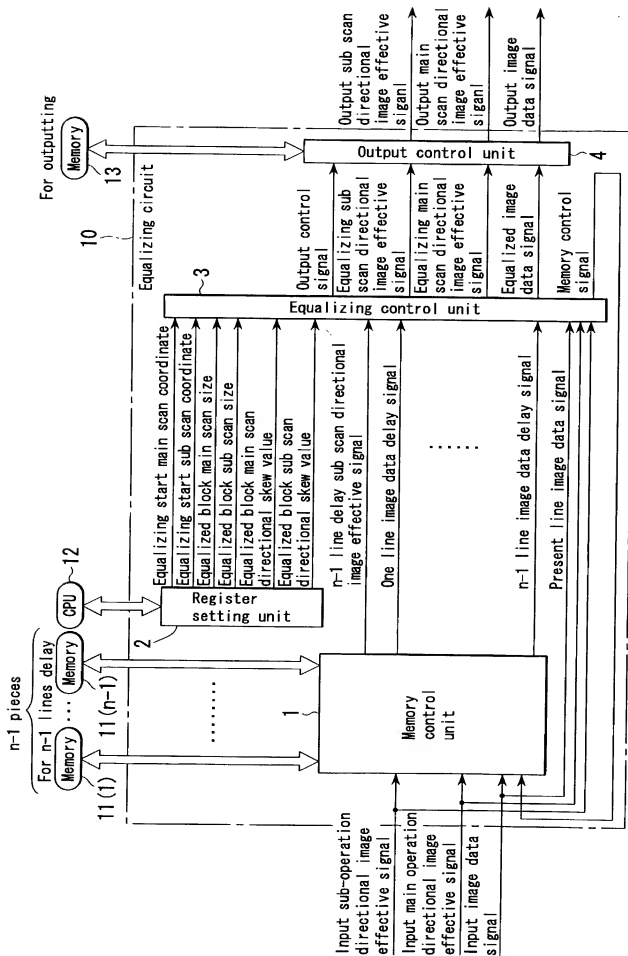


FIG. 5

Title: Equalizing Circuit And Method, And  
Image Processing Circuit And Method  
Inventor: Hiroki SATOH  
Appl. No.: 10/055,402

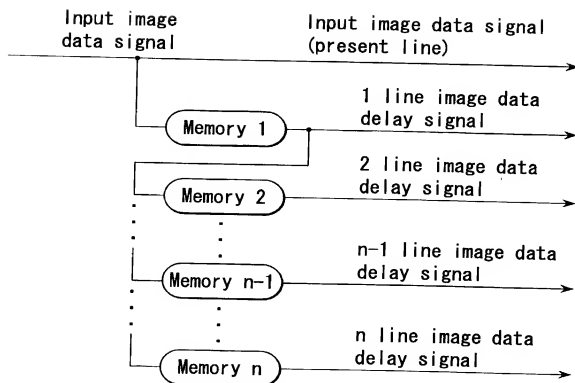
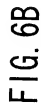


FIG. 6A





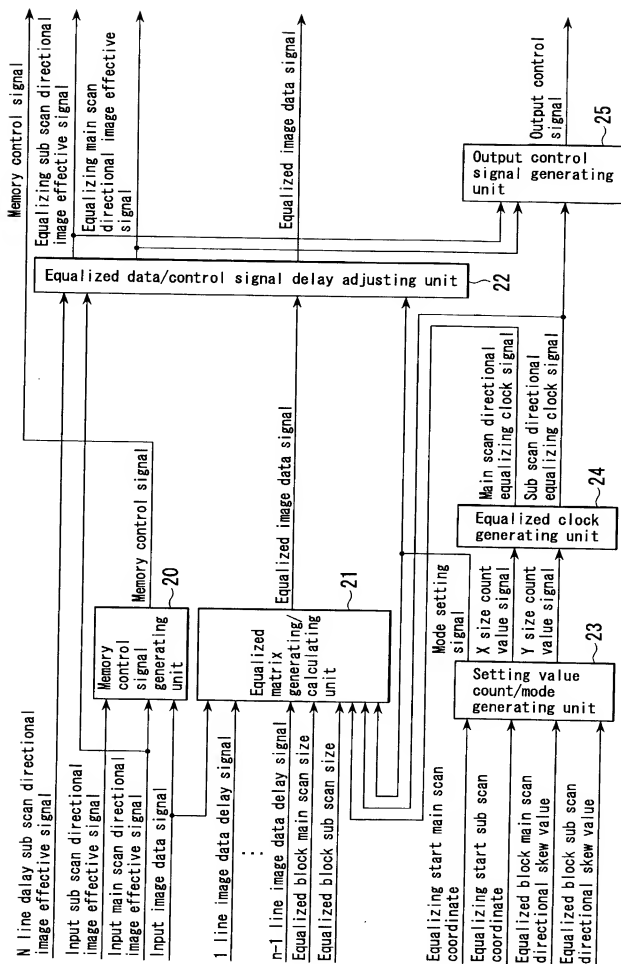


FIG. 7

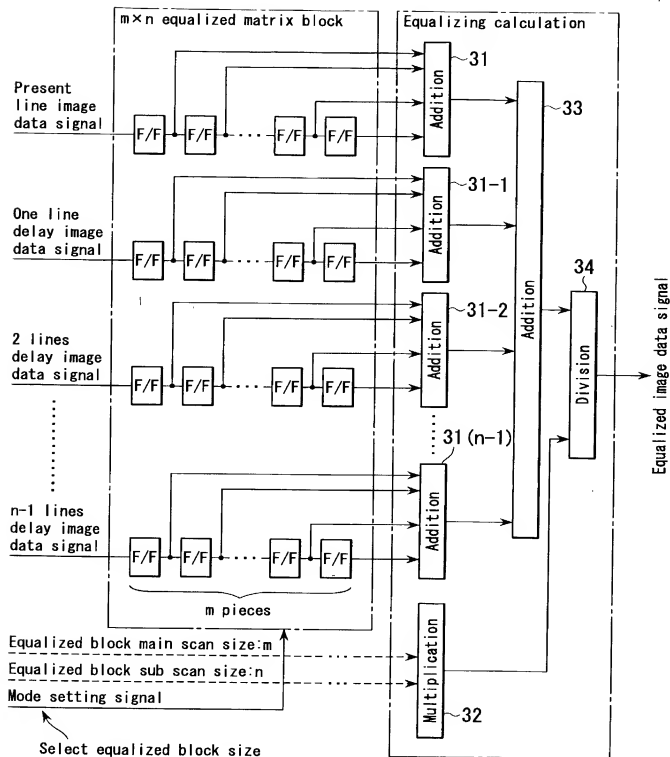
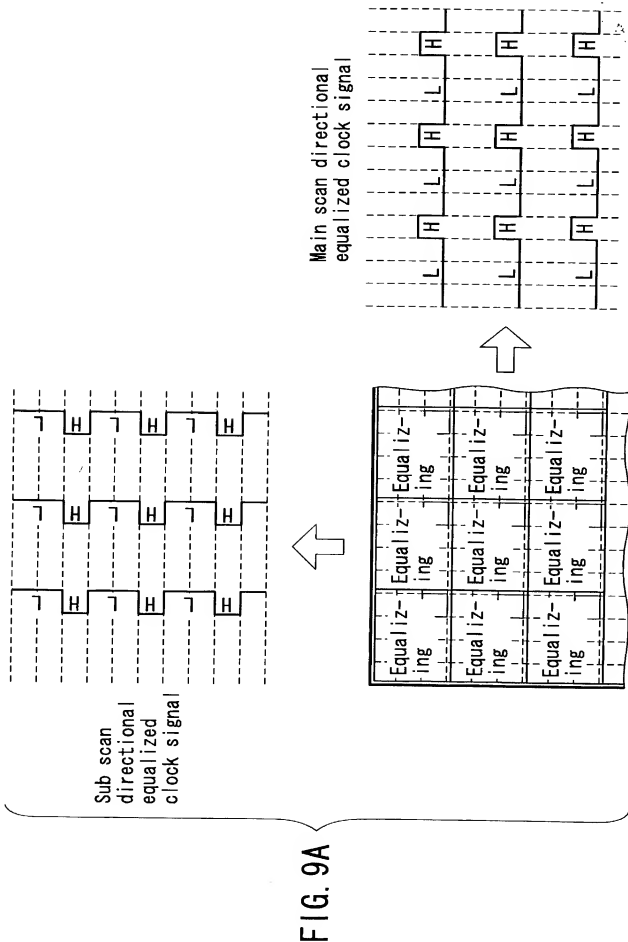


FIG. 8



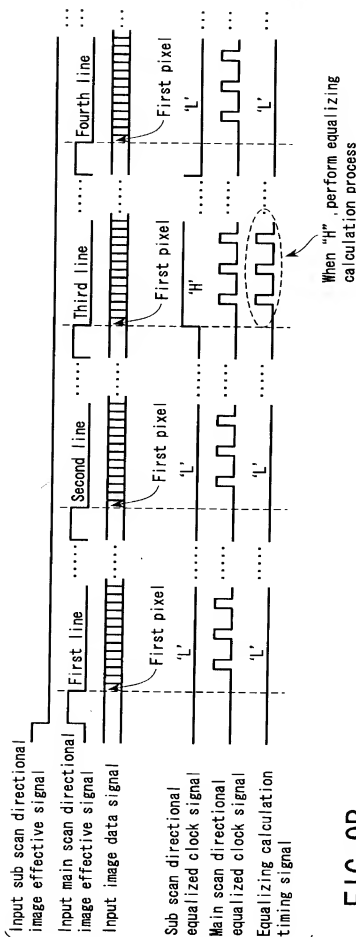


FIG. 9B

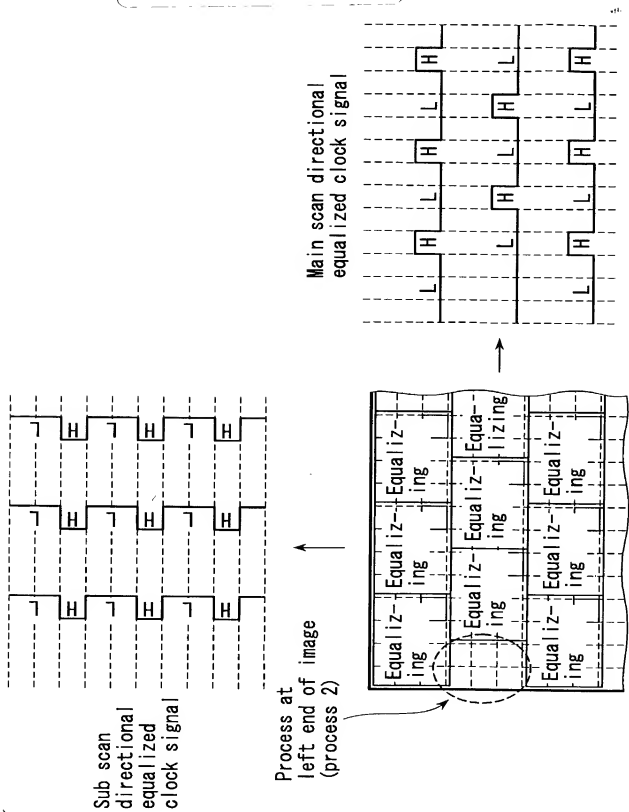
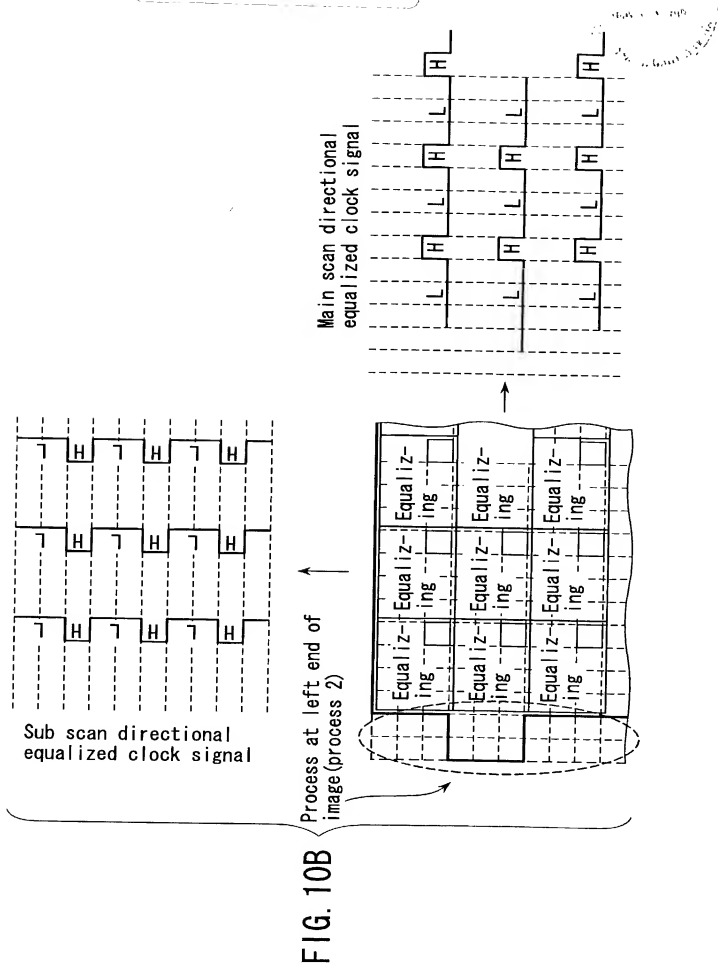


FIG. 10A



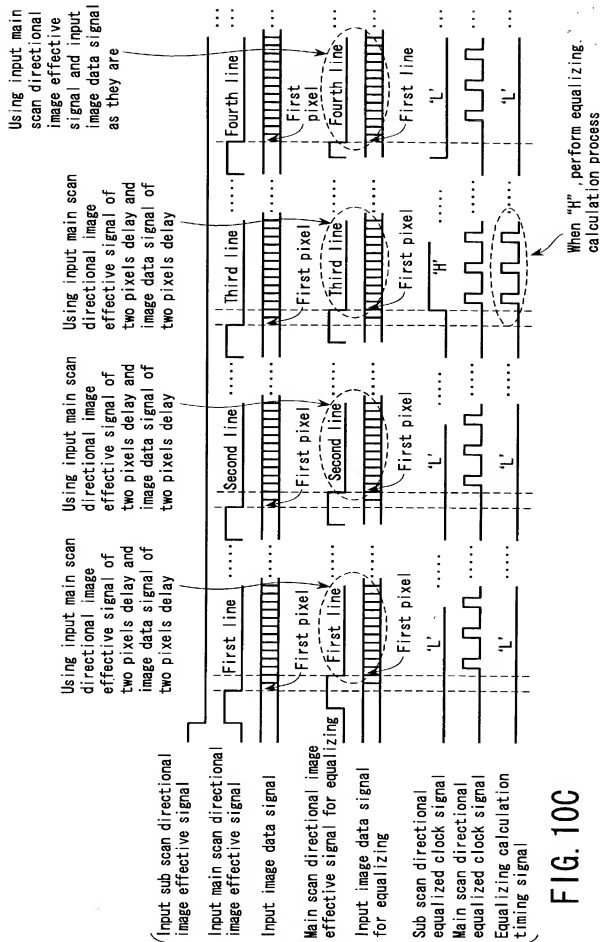


FIG. 10C





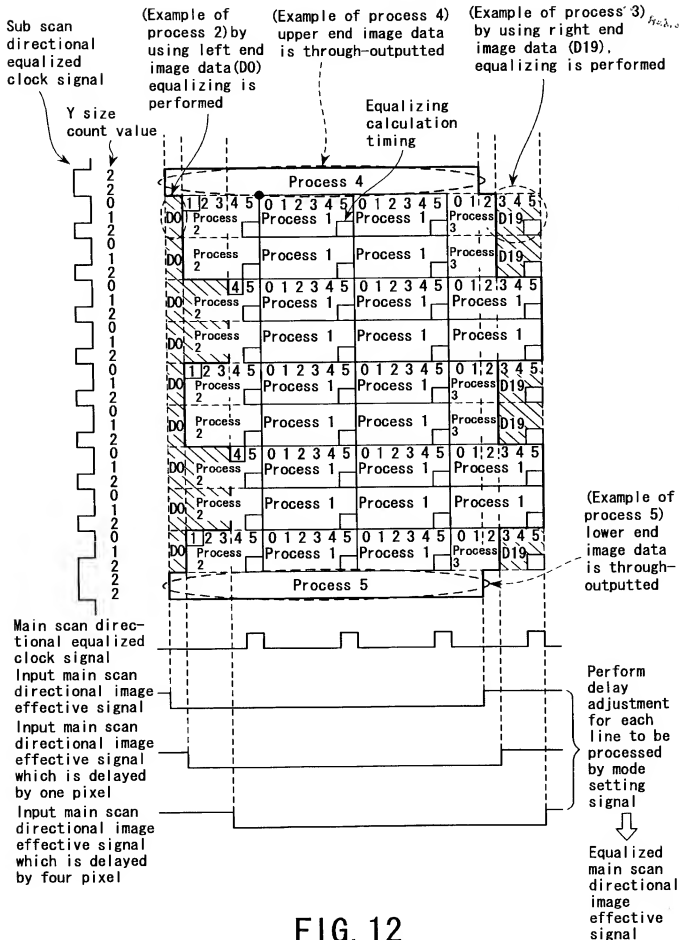


FIG. 12

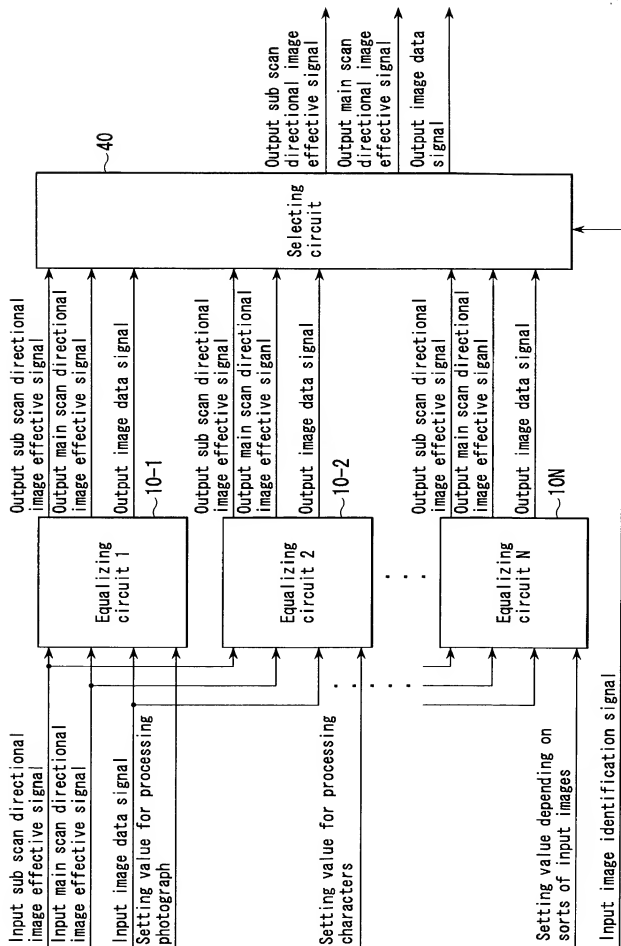


FIG. 13

Image are identified by this signal as photograph and characters

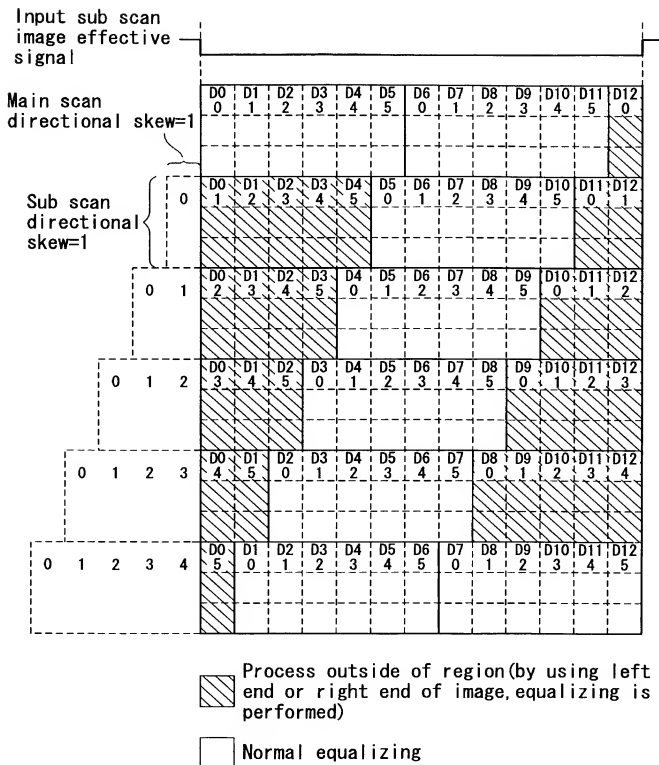


FIG. 14

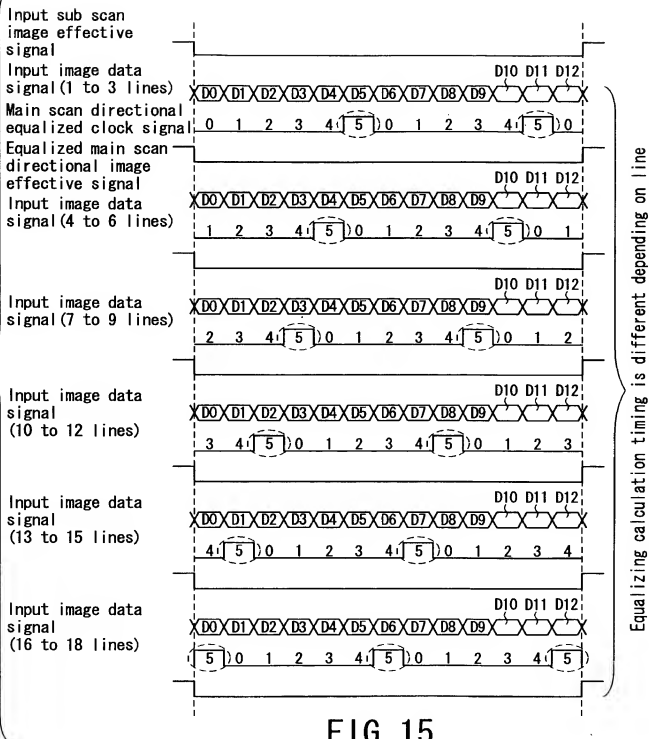


FIG. 15

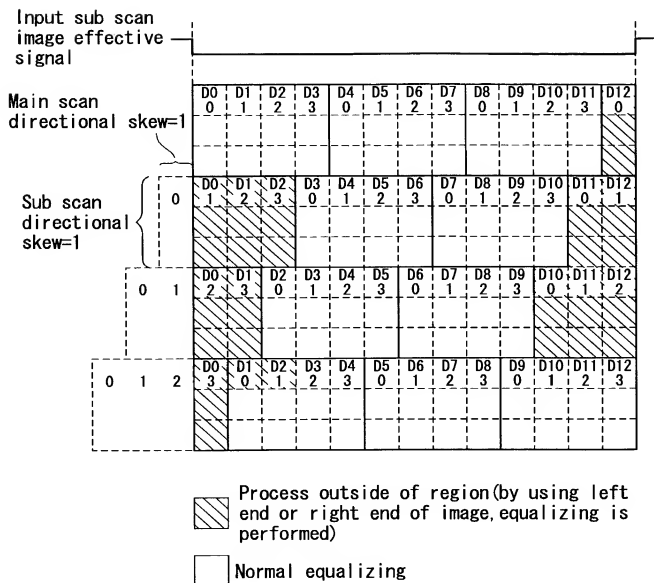


FIG. 16

Equalizing  
calculation  
timing is  
different  
depending  
on line

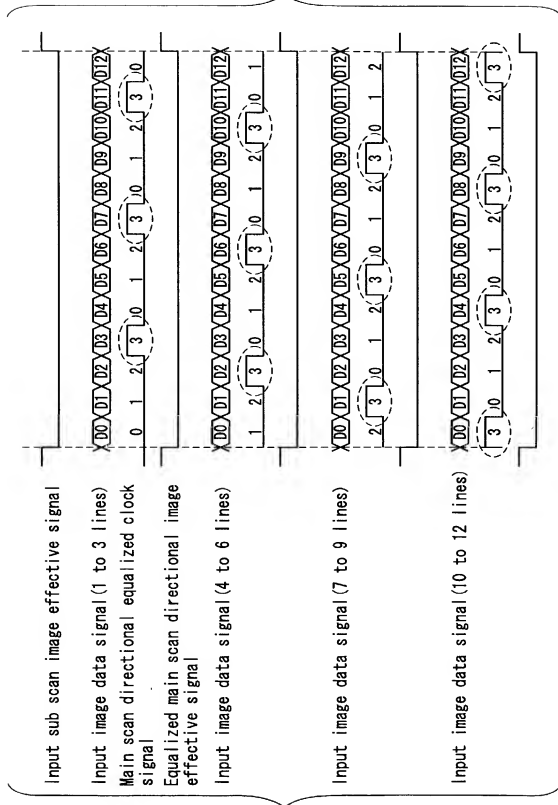
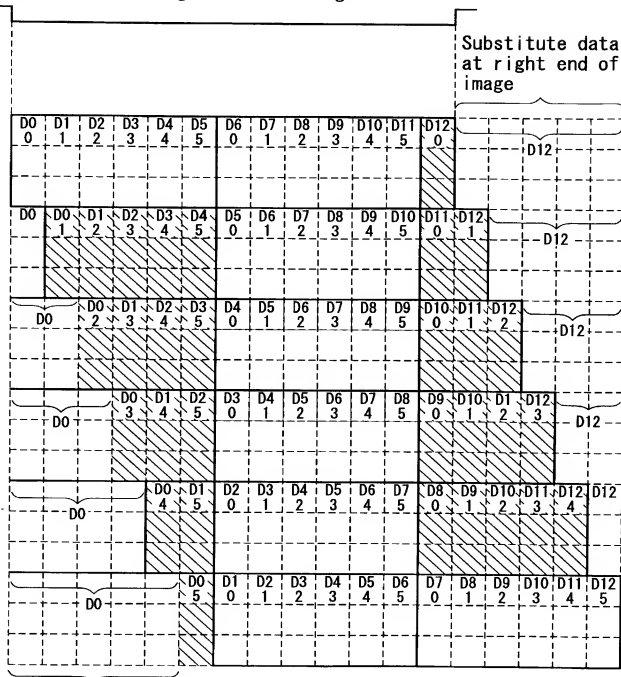


FIG. 17



Input sub scan image effective signal



Substitute data at  
left end of image

FIG. 18

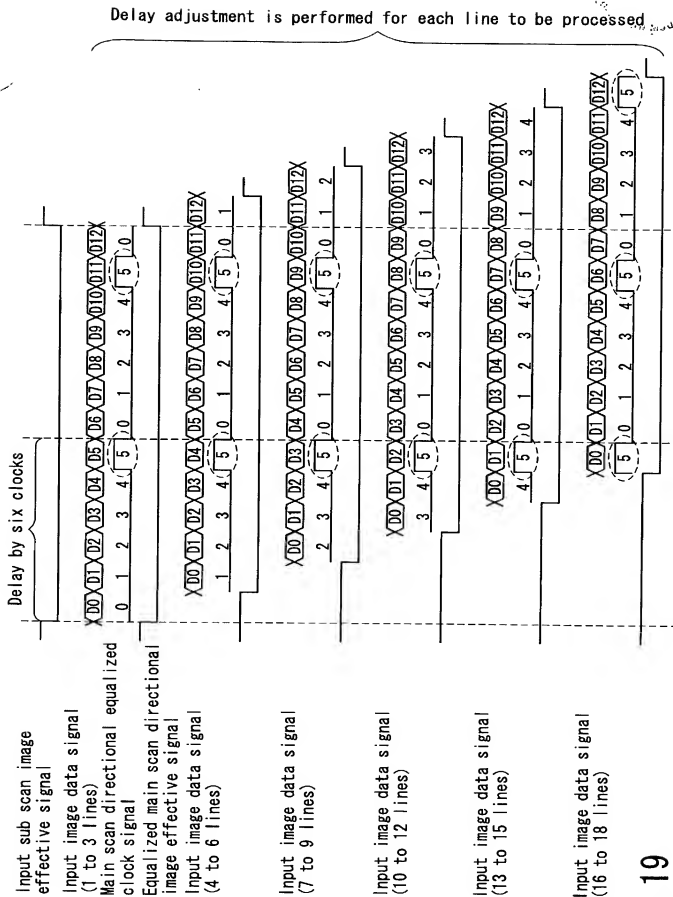


FIG. 19



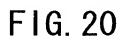


FIG. 20

~~X~~0~~X~~ 0~~X~~ 1~~X~~ 0~~X~~ 2~~X~~ 0~~X~~ 3~~X~~ 0~~X~~ 4~~X~~ 0~~X~~ 5~~X~~ 6~~X~~ 7~~X~~ 8~~X~~ 9~~X~~ 0~~X~~ 1~~X~~ 0~~X~~ 2~~X~~

---

0   1   2   3   0   1   2   3   0   1   2   3   0   1

---

~~X~~0~~X~~ 0~~X~~ 1~~X~~ 0~~X~~ 2~~X~~ 0~~X~~ 3~~X~~ 0~~X~~ 4~~X~~ 0~~X~~ 5~~X~~ 6~~X~~ 7~~X~~ 8~~X~~ 9~~X~~ 0~~X~~ 1~~X~~ 0~~X~~ 2~~X~~

---

1   2   3   0   1   2   3   0   1   2   3   0   1

---

~~X~~0~~X~~ 0~~X~~ 1~~X~~ 0~~X~~ 2~~X~~ 0~~X~~ 3~~X~~ 0~~X~~ 4~~X~~ 0~~X~~ 5~~X~~ 6~~X~~ 7~~X~~ 8~~X~~ 9~~X~~ 0~~X~~ 1~~X~~ 0~~X~~ 2~~X~~

---

2   3   0   1   2   3   0   1   2   3   0   1   2

---

~~X~~0~~X~~ 0~~X~~ 1~~X~~ 0~~X~~ 2~~X~~ 0~~X~~ 3~~X~~ 0~~X~~ 4~~X~~ 0~~X~~ 5~~X~~ 6~~X~~ 7~~X~~ 8~~X~~ 9~~X~~ 0~~X~~ 1~~X~~ 0~~X~~ 2~~X~~

---

2   3   0   1   2   3   0   1   2   3   0   1   2

---

~~X~~0~~X~~ 0~~X~~ 1~~X~~ 0~~X~~ 2~~X~~ 0~~X~~ 3~~X~~ 0~~X~~ 4~~X~~ 0~~X~~ 5~~X~~ 6~~X~~ 7~~X~~ 8~~X~~ 9~~X~~ 0~~X~~ 1~~X~~ 0~~X~~ 2~~X~~

---

3   0   1   2   3   0   1   2   3   0   1   2   3

---

~~X~~0~~X~~ 0~~X~~ 1~~X~~ 0~~X~~ 2~~X~~ 0~~X~~ 3~~X~~ 0~~X~~ 4~~X~~ 0~~X~~ 5~~X~~ 6~~X~~ 7~~X~~ 8~~X~~ 9~~X~~ 0~~X~~ 1~~X~~ 0~~X~~ 2~~X~~

---

3   0   1   2   3   0   1   2   3   0   1   2   3

---

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Input sub scan image effective
signal
Input image data signal
(1 to 3 lines)
Main scan directional equalized
clock signal
Equalized main scan directional
image effective signal
Input image data signal
(4 to 6 lines)

Input image data signal
(7 to 9 lines)

Input image data signal
(10 to 12 lines)

```

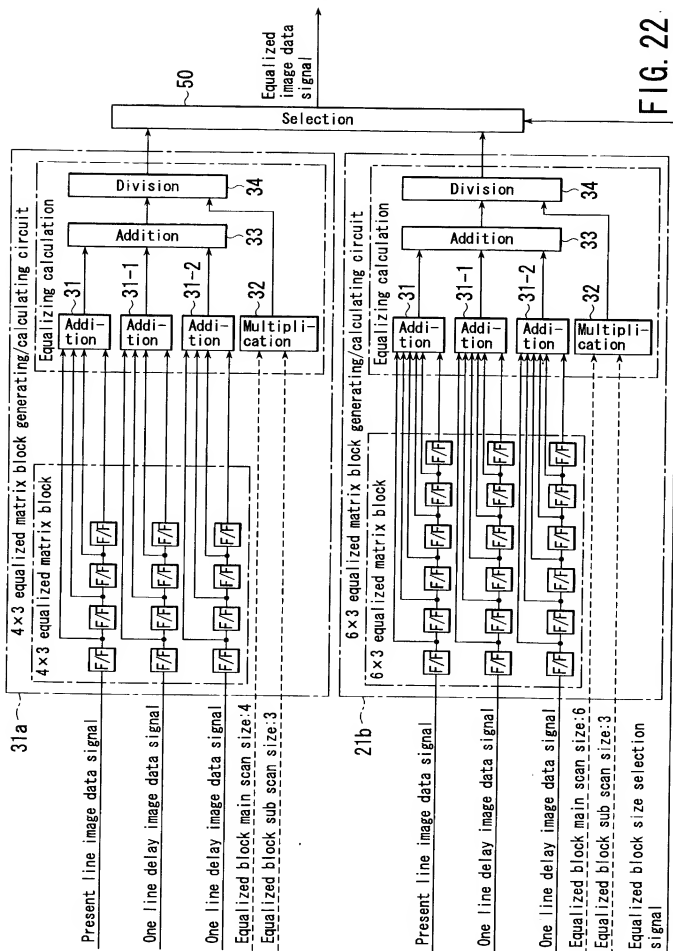


FIG. 22

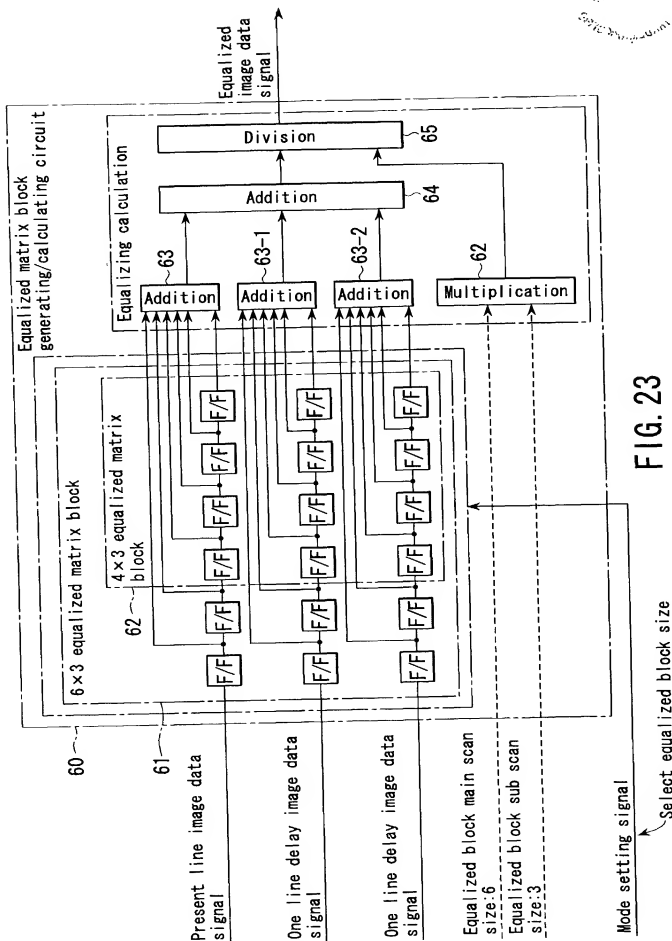


FIG. 23